

CLAIMS

What is claimed is:

- 1 1. A processing system comprising:
2 an application processor having a first graphics interface;
3 a coprocessor having a second graphics interface to communicate pixel-
4 stream formatted graphics command data and pixel-stream formatted image data
5 with the application processor, the coprocessor also having a display interface to
6 provide display data to a graphics display; and
7 a high-speed datapath between the first graphics interface and the second
8 graphics interface.
- 1 2. The processing system of claim 1 wherein the first graphics interface
2 comprises first drivers to receive graphics command data from a processing core
3 of the application processor and to format the graphics command data into the
4 pixel-stream formatted graphics command data,
5 wherein the second graphics interface comprises second drivers to
6 reformat the pixel-stream formatted graphics command data back to the graphics
7 command data,
8 wherein the first drivers and the second drivers comprise at least one of
9 either hardware or software components, and
10 wherein the high-speed datapath comprises a pair of conductors to carry
11 high-speed digital differential signals.
- 1 3. The processing system of claim 1 wherein the coprocessor further
2 comprises a coprocessor processing core responsive to the graphics command data
3 and image data to generate the display data for the graphics display.
- 1 4. The processing system of claim 1 wherein the coprocessor comprises a
2 graphics accelerator to offload at least some graphics-processing operations from
3 the application processor, the graphics-processing operations including at least
4 one of two-dimensional (2D) graphics operations, three-dimensional (3D)

5 graphics operations, multimedia encoding and decoding operations, and display
6 refresh operations, the at least some graphics-processing operations indicated by
7 the graphics command data.

1 5. The processing system of claim 1 wherein the graphics command data
2 comprises commands to instruct the coprocessor to perform graphics-processing
3 operations including at least one of two-dimensional (2D) graphics operations,
4 three-dimensional (3D) graphics operations, multimedia encoding and decoding
5 operations, and display refresh operations.

1 6. The processing system of claim 1 further comprising a system bus and a
2 system memory, wherein the application processor has a memory controller to
3 access the system memory over the system bus, and wherein the coprocessor has a
4 system memory interface to access the system memory over the system bus.

1 7. The processing system of claim 6 wherein the application processor
2 further comprises on-die memory therein, the application processor performs a
3 DMA transfer of graphics data from the on-die memory to the coprocessor over
4 the high-speed datapath, and the application processor refrains from transferring
5 the graphics data to the coprocessor over the system bus.

1 8. The processing system of claim 1 wherein the coprocessor is an
2 integrated part of the graphics display.

1 9. The processing system of claim 8 wherein the graphics display
2 comprises photodiodes to generate image data of a scanned image, and the
3 coprocessor converts the image data to pixel-stream formatted image data for
4 transfer over the high-speed datapath to the application processor.

1 10. The processing system of claim 1 wherein the display data describes
2 pixels of the graphics display in a per-pixel format, and wherein the pixel-stream
3 formatted image data comprises pixel data in a pixel format, and wherein the
4 pixel-stream formatted command data comprises command data in a pixel format.

1 11. The processing system of claim 1 wherein the coprocessor comprises
2 one of a graphics accelerator, a hardware accelerator, or a companion device.

1 12. The processing system of claim 1 further comprising:
2 an omnidirectional antenna to receive communication signals; and
3 a receiver to translate the communication signals to data signals for the
4 application processor, the communication signals including graphics data,
5 the application processor generates the graphics command data from the
6 received graphics data, and transfers the pixel-stream formatted graphics
7 command data over the high-speed datapath to the coprocessor, the coprocessor
8 reformats the pixel-stream formatted graphics command data and generates
9 display data for display by the graphics display.

1 13. The processing system of claim 12 comprising one of either a personal
2 digital assistant (PDA) or a wireless telephone.

1 14. The processing system of claim 1 comprising a general processing
2 system.

1 15. A communication device comprising:
2 an application processor having a first interface;
3 a coprocessor having a second interface to receive formatted command
4 data and formatted output data from the application processor, the coprocessor
5 also having an output interface to provide output data to an I/O device; and
6 a high-speed datapath to communicate the formatted command data and
7 formatted output data between the first interface and the second interface.

1 16. The device of claim 15 wherein the first interface comprises first
2 drivers to receive command data from a processing core of the application
3 processor and to format the command data into the formatted command data,
4 wherein the second interface comprises second drivers to reformat the
5 formatted command data back to the command data,

6 wherein the first drivers and the second drivers comprise hardware and
7 software components, and

8 wherein the high-speed datapath comprises a pair of conductors to carry
9 high-speed digital differential signals.

1 17. The device of claim 15 wherein the coprocessor further comprises a
2 coprocessor processing core responsive to the command data and output data to
3 generate the output data for the I/O device.

1 18. The device of claim 15 further comprising a system bus and a system
2 memory, and wherein the application processor has a memory controller to access
3 the system memory over the system bus, and wherein the coprocessor has a system
4 memory interface to access the system memory over the system bus.

1 19. The device of claim 18 wherein the application processor further
2 comprises on-die memory, the application processor performs a DMA transfer of
3 data from the on-die memory to the coprocessor over the high-speed datapath, and
4 the application processor refrains from transferring the data to the coprocessor
5 over the system bus.

1 20. The device of claim 15 wherein the I/O device includes RF circuitry to
2 interface with an antenna for communication of RF signals, the application
3 processor and coprocessor communicate at least one or either digitally encoded
4 data or digitally encoded voice signals over the high-speed datapath, wherein
5 wireless transceiver functions are allocated between the applications processor and
6 the coprocessor for wireless communications.

1 21. A method comprising:
2 formatting graphics command data into a pixel-stream format;
3 sending the pixel-stream formatted graphics command data along with
4 pixel-stream formatted image data from a first graphics interface of an application
5 processor over a high-speed datapath to a second graphics interface of a
6 coprocessor;

7 reformatting the pixel-stream formatted graphics command data at the
8 coprocessor back to graphics command data; and
9 generating, by the coprocessor, display data for a graphics display from the
10 graphics command data and image data received over the high-speed datapath.

1 22. The method of claim 21 further comprising, prior to sending, buffering
2 the pixel-stream formatted graphics command data, and wherein sending
3 comprises programming a DMA descriptor to send the pixel-stream formatted
4 graphics command data from the buffer along with pixel-stream formatted image
5 data to the coprocessor.

1 23. The method of claim 21 further comprising refraining, by the
2 application processor, from sending the graphics command data along with pixel-
3 stream formatted image data to the coprocessor over a system bus.

1 24. The method of claim 21 wherein generating display data comprises
2 performing graphics-processing operations including at least one of two-
3 dimensional (2D) graphics operations, three-dimensional (3D) graphics
4 operations, multimedia encoding and decoding operations, and display refresh
5 operations.

1 25. A communication system comprising:
2 an omnidirectional antenna to receive communication signals;
3 a receiver to translate the communication signals to data signals; and
4 a processing system having an application processor and a coprocessor
5 coupled by a high-speed datapath,
6 wherein the application processor receives the data signals and generates
7 and sends data-stream formatted graphics command data and data-stream
8 formatted image data to the coprocessor over the high-speed datapath, the
9 coprocessor having a display interface to generate and to provide display data for a
10 graphics display.

1 26. The system of claim 25 wherein the first graphics interface comprises
2 first drivers to receive graphics command data from a processing core of the
3 application processor and to format the graphics command data into the data-
4 stream formatted graphics command data,
5 wherein the second graphics interface comprises second drivers to
6 reformat the data-stream formatted graphics command data back to the graphics
7 command data,
8 wherein the first drivers and the second drivers comprise at least one of
9 either hardware or software components, and
10 wherein the high-speed datapath comprises a pair of conductors to carry
11 high-speed digital differential signals.

1 27. The system of claim 25 wherein the coprocessor further comprises a
2 coprocessor processing core responsive to the graphics command data and image
3 data to generate the display data for the graphics display.

1 28. The system of claim 25 wherein the coprocessor comprises a graphics
2 accelerator to offload at least some graphics-processing operations from the
3 application processor, the graphics-processing operations including at least one of
4 two-dimensional (2D) graphics operations, three-dimensional (3D) graphics
5 operations, multimedia encoding and decoding operations, and display refresh
6 operations, the at least some graphics-processing operations indicated by the
7 graphics command data.